IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: KIM et al Serial No.: 10/804,430 Filed: March 19, 2004 Title: METHOD FOR THE OPTIMIZATION OF SUBSTRATE ETCHING IN A PLASMA PROCESSING SYSTEM	Group Art Unit: 1765 Examiner: UNASSIGEND Docket: P1205/LMRX-P032 Confirmation No.: 7228

INFORMATION DISCLOSURE STATEMENT

OTHER DOCUMENTS

Examiner Initials	Cite No.		T
LV	1	Yeoh et al., "Photoresist Strip on Orion2.2™ in Via First Dual Damascene Cu Structures", Trikon Technologies, Ringland Way, Newport, South Wales, http://www.trikon.com/lowk/avs_2002_yeoh_abstract.pdf	
	2	Hu et al., "Resist Stripping for Multilevel Interconnect Integrating Low-k Dielectric Material", February 2000, AVS First International Conference on Microelectomics and Interfaces	
	3	Chhambra et al., "Interconnect Challenges and Strategic Solutions", February 2, 2002, Future Fab Intl. Volume 12, Issue 17, http://www.future-fab.com/documents.asp?d_ID=912	
	4	Singer, Peter, "Dual-Damascene Challenges Dielectric Etch", August 1999, Semiconductor International, http://www.semipark.co.kr/upload1/Dual-Damascene%20Challenges%20Dielectric%20Etch.pdf	
	5	Schmid et al., "A Novel Oxazole Based Low k Dielectric Addresses Copper Damascene Needs", Semiconductor Fabtech 12th edition, pp. 231-235, http://www.semiconductorfabtech.com/journals/edition.12/fabtech12.pdfs/ft12_pg231.pdf	
	6	Peters, Laura, " Solving the Integration Challenges of Low-k Dielectrics", November 1999, Semiconductor International 22, No. 13, pp. 56-64.	
	7	Lassig et al., "Selective Removal Strategies for Low k Dual Damascene", December 2001, Semiconductor Fabtech Edition 15, pp. 185-190	
	8	Ramalingam et al., "Photoresist Trimming: Etch Solutions to CD Uniformity and Tuning", September 2002, Semiconductor International Volume 20, Issue 5	
	9	Wolf, "Overview of Dual Damascene Cu/Low-k Interconnect", August 2003, International SeMaTech	
LV	10	Mo Koo, "Design and Process Issues of Junction- and Ferroelectric- Field Effect Transistors in Silicon Carbide", 2003, KTH, Royal Institute of Technology Department of Microelectronics and Information Technology Device Technology Laboratory, ISRN KTH/EKT/FR-2003/1-SE	

Examiner Signature		Date Considered	11/7/05

ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

Title of Invention	Methods for the optimization of substrate etching in a plasma processing system

Application Number : 10/804430

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First Named Applicant: Jisoo Kim

Attorney Docket Number: LMRX-P032/P1205

Art Unit: 1765

Examiner: Nadine G Norton

Search string: (6518174).pn

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
LV	1	6518174	2003-02-11	Annapragada, et al.			

Signature

Examiner Name	Date
LAN VINH	11/7/05